



The Compact Muon Solenoid Experiment

**ECAL** Electromagnetic CALorimeter

# **Design Guidelines For Implementation of Boundary Scan in the ECAL/HCAL Crates**

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## Boundary Scan Implementation at Crate Level

The implementation of boundary scan at crate level proposed here includes the boundary scan implementation at each board or subsystem and the dedicated logic for the control of the boundary scan operations in the crate. Fig. 3 shows the general architecture of the system.

The **Boundary Scan Crate Controller** is a block of logic responsible for the application of the test/programming vectors to a specific board or subsystem. In the ECAL ULRT trigger crates this controller will be implemented in the DCC-MB board.

The application of the test/programming vectors is performed through the **MTM Test lines**, which are included in the VME64x backplane. The MTM lines are used as standard 1149.1 test lines from the tester (BS Crate Controller) point of view.

Each **Board Under Test** or **Sub-System** connected to the VME backplane, interfaces the MTM lines through a dedicated circuit named Scan Bridge. This addressable circuit allows the partition of the local scan chains located in each board/sub-system. The test architecture at board/sub-system (Scan Bridge and local scan chains) is also used in the same physical board housing the BS Crate Controller, allowing the board to be tested in a backplane system.

A prototype 6U slave board housing the BS Crate Controller was implemented and tested with success in the ECAL group. A test board with a single Scan Bridge interfacing an external connector, and with a local scan chain, was also tested. The backplane architecture proposed in this document, which uses the MTM test lines for application of the test vectors, is under implementation at this moment.

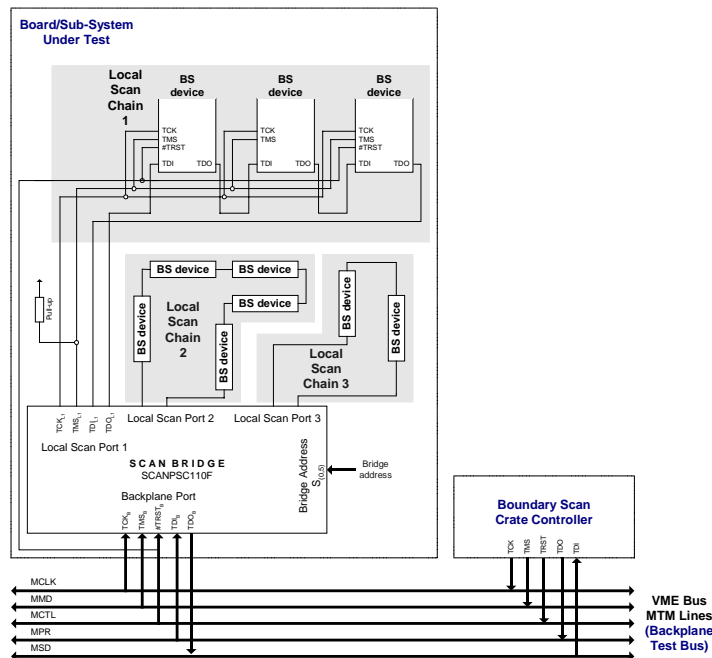


Fig. 3 – Boundary Scan architecture at crate level.

## The Boundary Scan Crate Controller

In the ECAL ULRT crates this controller will be implemented in the DCC-MB board and it will control the application of boundary scan operations in each board in the crate and in the DCC itself. The controller is accessed using the DCC VME interface and drives the 5 MTM test signals in the VME backplane. Fig. 4 shows the proposed circuits for the implementation of the controller. A similar architecture was used with success in a prototype board developed for ECAL.

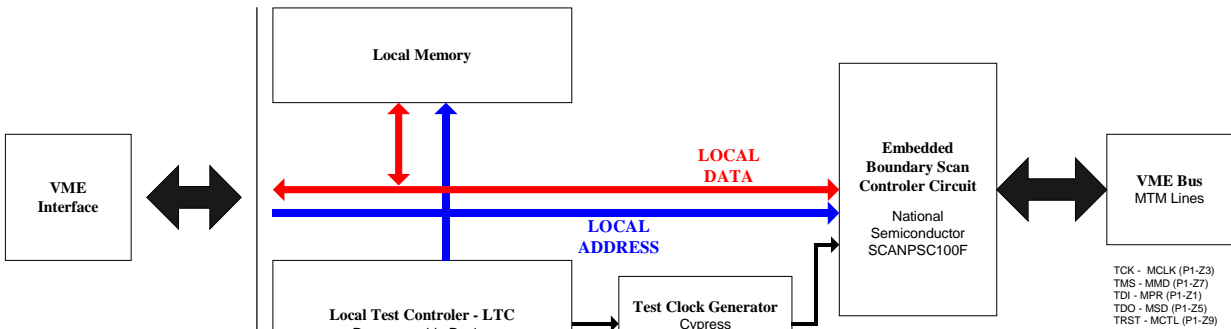


Fig. 4 – Boundary Scan Crate Controller.

### 1 - Local Test Controller Circuit

The Local Test Controller (LTC) is the circuit responsible for controlling the functionality of the BS Crate controller, during the execution of boundary scan operation. This circuit interfaces the local circuits and the VME interface. A programmable logic device from Altera was used to implement the designed functionality in a prototype board.

### 2 - Local Memory

A local SRAM memory for storing the test vectors and the test results is included in the controller. This local memory should be large enough to store the amount of data necessary for application of boundary scan tests and for in-circuit programming. In a boundary scan prototype board we used 4 banks of memory, each with 128 K x 8 bits, 4Mbits total. This amount of memory was more than sufficient for storing the boundary scan tests.

### 3 - Test Clock Generator

The Test Clock Generator generates the boundary scan test clock applied to the TCK signal. The Cypress ICD2053 was used to generate the test clock signal. This circuit is configured to generate a clock output with frequency ranging from 391 Hz to 100 MHz. The circuit possesses two dedicated input pins, a serial clock input (SCLK) and a serial data input (DATA) for programming the output frequency. The necessary algorithm for programming the circuit is implemented in the Local Test Controller circuit.

## 4 - Embedded Boundary Scan Controller Circuit

The SCAN PSC100F, Embedded BS Controller circuit manages the operation of the test shifters/buffers that connect to the backplane JTAG test signals, TDO, TMS, TDI and TCK – Fig. 5. For each active test signal, there is a double-buffered parallel/serial shift register (2 X 8 bits FIFO) or Shifter/Buffer. This double buffering allows the parallel write/read to/from one of the 8-bit FIFOs of the shifter/buffer, while the other is shifting data to/from the scan chain. Three Shifter/Buffers are provided for outgoing serial data (TDO, TMS0 and TMS1) and one is provided for incoming serial data (TDI).

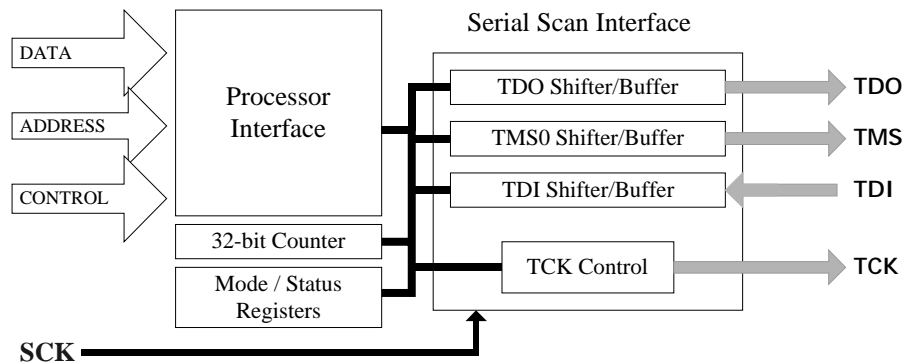


Fig. 5 – Embedded Boundary Scan Controller circuit.

The optional TRST signal, if implemented must be generated by an external circuit.

## 5 - External Boundary Scan Connector

For applying the boundary scan vectors to an external system, not residing in the VME backplane, it could help to include in the BS Crate Controller an external connector (not shown in figure). The proposed pinout for this connector is shown in Fig. 10 and table 2 (TDI, pin 5 and TDO, pin 3 connect to the TDO and TDI pins respectively, of the Embedded BS Controller Circuit).

## The Backplane Test Bus

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The VME64x extension of the VME architecture specifies 5 test lines to be used for system testing. These lines are grouped in the Module Test and Maintenance (MTM) bus. This bus allows the test of the system boards and is included in the P1/J1 connector/slot. The lines in this bus will be used as standard JTAG 1149.1 test lines.

Table 1 shows the correspondence of JTAG signal names into MTM signal names, together with the corresponding VME connector pin.

JTAG Signal (Scan Bridge pin)	MTM Line	VME P1/J1 Pin
TMS (TMS <sub>B</sub> )	MMD	Z7
TDI (TDI <sub>B</sub> )	MPR	Z1
TDO (TDO <sub>B</sub> )	MSD	Z5
TCK (TCK <sub>B</sub> )	MCLK	Z3
#TRST (#TRST)	MCTL	Z9

**Table 1** – JTAG-to-MTM conversion table.

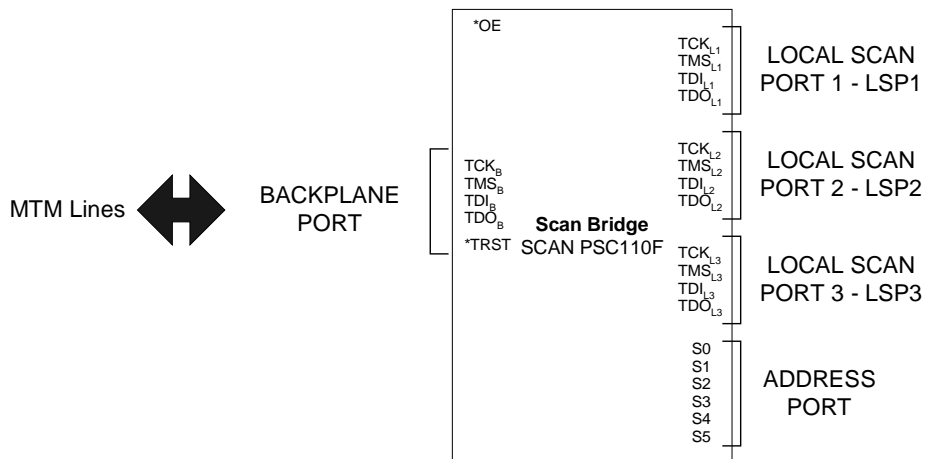
**NOTE:** TDI connects to the Scan Bridge backplane TDI, in the board under test.  
TDO connects to the Scan Bridge backplane TDO, in the board under test.

## Boundary Scan at Board/Sub-System Level

### 1 - Scan Bridge

The SCAN PSC110F Scan Bridge performs the interface between the MTM test lines and the boundary scan chains in each board. This device includes a *backplane port* and 3 *local scan ports* - Fig. 6.

The backplane port interfaces the boundary scan test signals in the backplane (the MTM lines). The local scan ports interface up to 3 local boundary scan chains, which can be accessed individually or combined serially.



**Fig. 6** – Scan Bridge.

Unlike other approaches the PSC110F provides an addressing scheme using 1149.1 compatible protocol. This addressing scheme allows the individual selection of each PSC110F in a backplane system and the use of 1149.1 boundary scan software. The Scan Bridge device possesses a 6-bit address port that specifies its address in the test backplane. This address must be different for each Scan Bridge in the same backplane and could be obtained, for example, from the board address.

## Local Scan Ports

The Local Scan Port Network (LSPN) contains multiplexing logic used to select different port configurations. The LSPN block contains the Local Scan Port Controllers (LSPC) for each Local Scan Port (LSP1, LSP2 and LSP3). Each of the LSPs has four signals,  $TDI_{L(1-3)}$ ,  $TDO_{L(1-3)}$ ,  $TMS_{L(1-3)}$  and  $TCK_{L(1-3)}$ , that drive the local scan chains formed by the boundary scan circuits. The PSC110F has a total of 5 state machines, and three of them are used to control the insertion of local scan ports into the overall scan chain, or the isolation of the local ports from the chain. This separation of the boundary scan circuits allows the simplification of the test generation and offers more flexibility to the board designer.

## 2 - Local Chain Design

The design of the boundary scan test architecture should take into account the possibilities offered by the Scan Bridge and the restrictions posed by the software for generation of the test vectors and programming vectors.

The generation of test vectors is performed automatically by an ATPG integrated into the JTAG Technologies test software, available at CERN. The ATPG uses the information about the chain architecture and the BS circuits to generate the necessary test vectors without any user interaction. Once generated the test vectors cannot be modified. Therefore the chosen architecture should be fully accepted by the test tools.

## Boards with Piggyback or Plug-in Boards

Consider the architecture shown in Fig. 7 in which 2 piggyback or plug-in boards (secondary boards) and a transition board connect to a main board, interfacing the VME backplane. All boards have boundary scan testable circuits. This sub-system is formed by four boards with the main board containing the Scan Bridge device for test interface.

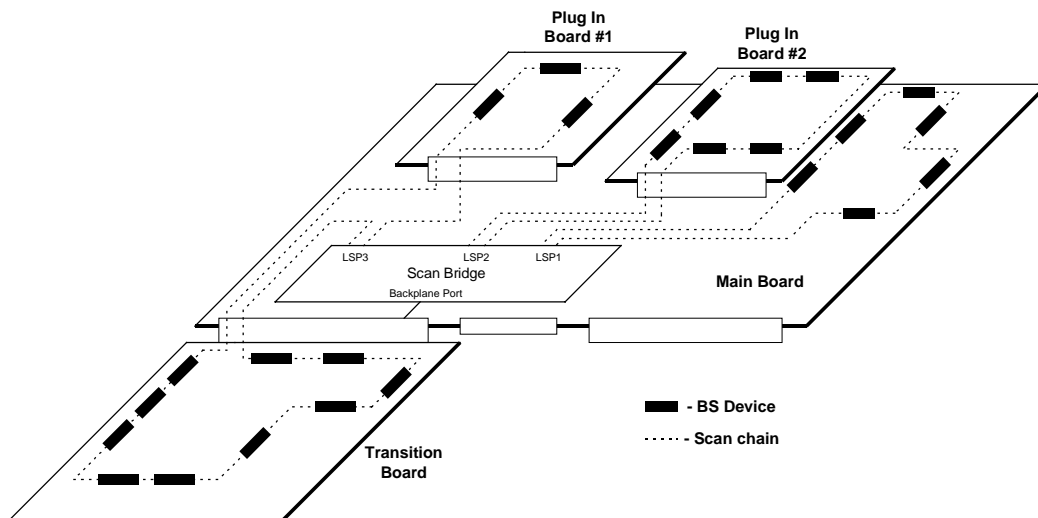


Fig. 7 – Board architecture – example 1.

If it is required to test interconnections between the main board and the plug-in boards, then, all local scan chains should be connected to the same Scan Bridge. In this case the following rules should be applied.

- 1) Use LSP1 for the boundary scan circuits residing in the main board, independently of boundary scan operations performed by the circuits (programming and/or testing).
- 2) Use a different LSP for each plug-in board.

When the number of LSPs is not enough as it is shown in Fig. 7 where we have 2 plug-in boards and one transition board, then two cases are possible:

- 1) There are interconnections between the transition board and the main board and/or the plug-in boards for being tested with boundary scan. In this case one of the chains (LSP3 in the figure) must be serially connected through 2 secondary boards. It should be noticed that with this connection it is not possible to test the local scan chain 3 when the transition board is not connected.
- 2) There are no boundary scan testable interconnections between the transition board and/or the plug-in boards. In this case use another Scan Bridge for the transition board.

During test generation a netlist merger merges the boards netlists into a single drop netlist. This netlist that can be used by the test generator for generating the test vectors for testing the interconnections involving all the boards.

## **Single Main Boards**

In a main board without plug-in boards, the LSPs should interface the boundary scan circuits accordingly with the boundary scan operations performed by the circuits. It is also preferable to divide the BS in-circuit-programmed circuits into several chains. This allows the simplification of test generation and the reduction of the total programming time necessary for in-circuit programming. As a rule:

- 1) The boundary scan circuits only for test should be placed in a different scan chain – Testing Chain. Use LSP1 for the Testing Chain.
- 2) The circuits for boundary scan in-circuit programming (and testing) should be placed in a separate scan chain – designated Programming Chain. Divide the BS in-circuit-programmed devices into the remaining chains. Use LSP2 and LSP3 for the Programming Chains (Fig. 8) or LSP2, LSP3 and LSP1 if no BS circuits for testing exist.

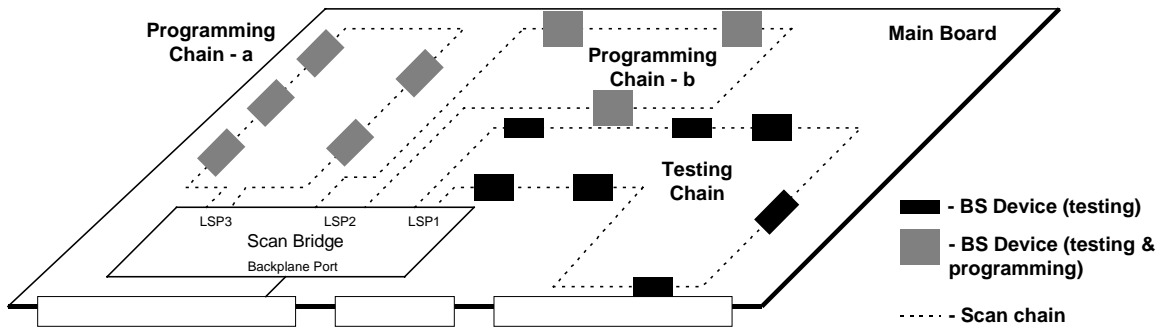


Fig. 8 – Board architecture – example 2.

### 3 - Access to a Local Chain Bypassing the Scan Bridge

For accessing a local scan chain using an external BS controller, bypassing the Scan Bridge, it is possible to interface a connector directly to the scan chain by using the OE pin available in the Scan Bridge. When this pin is in the high level the local port signals are placed in high impedance, allowing access to a local scan chain, as it is shown in Fig. 9.

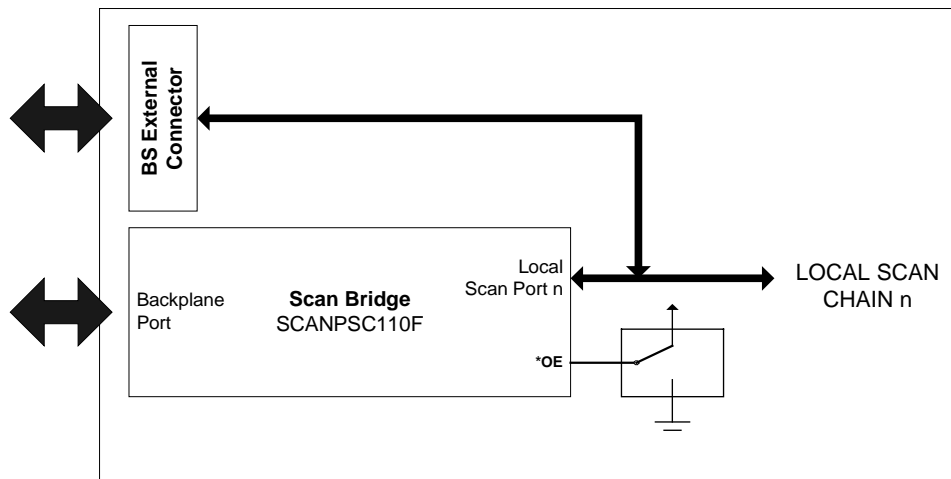


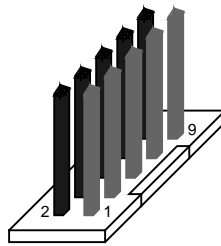
Fig. 9 – Access to a local scan chain using an external connector.

Table 2 and Fig. 10 show the connections for the proposed boundary scan access connector, located in each the board under test.

JTAG Signal	Connector Pin
TMS	7
TDI	5
TDO	3
TCK	9
TRST	1
Ground	2 to 10

**Table 2** – Pinout of the boundary scan access connector.

**NOTE:** TDI connects to the local chain TDI.  
TDO connects to the local chain TDO.



**Fig. 10** - Proposed boundary scan access connector, 10-pin flat cable male connector.

The local chains containing programmable circuits should be directly accessible, without the Scan Bridge, when an external system (for example XILINX JTAG Programmer + Parallel Cable or ALTERA JTAG Programmer + Download Cable) is used to directly program the chain devices. This is due to the fact that the Scan Bridge, although a BS device, is not recognized by these software tools.

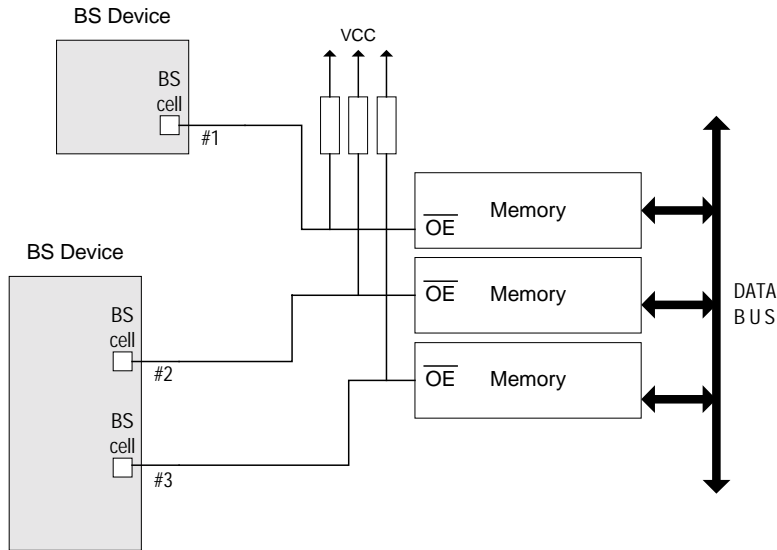
## **A Few Design for Testability Guidelines**

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### **1 - Bus Contention**

Some care must be taken when designing a digital board with boundary scan infrastructure. During boundary scan operations the BS circuits operate in test mode and therefore their system logic, or the normal operation logic, is disabled (this is true for most test modes). This means that the logic signals controlled by this logic are left without control.

During test mode, the BS circuits are disabled which leaves the memory circuits connected to the data bus in a contention situation if no care is taken with their output enable pins. It is advisable to include pull-up or pull-down resistors in Output enables driven by BS circuits in order to disable the correspondent drivers when the BS circuits are under boundary scan control, as it is shown in figure 11.

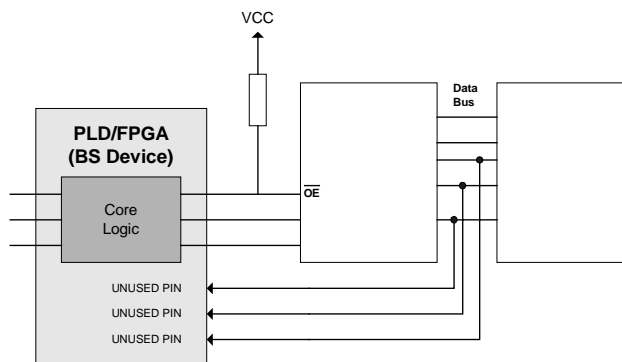


**Fig. 11** – Use of disabling resistors for avoiding data bus contention.

Avoid placing control pins, such output enables and direction pins, in a constant level using only pull-ups or pull-downs. If possible connect them also to an unused BS programmable device even if their stat remains unchanged during normal operation.

## 2 - PLD/FPGA Unused Pins

Each pin of a boundary scan circuit represents a driving/sensing cell that can be used to observe and/or stimulate a net. The test coverage can be increased by connecting unused pins of programmable logic devices to important nets of the board under test, as it is shown in Fig. 13. These pins should be connected to important signals in the test board such as control pins, primary logic cluster (blocks of non-BS logic) input/output pins, data pins. These connections should be included in the board netlist.



**Fig. 12** – Connection of unused PLD/FPGA pins.

### **3 - Boundary Scan Buffers and Transceivers**

Introducing circuits that provide access to data, address and control lines can increase the test coverage substantially. When these circuits operate in no-boundary scan mode they behave as transceivers or buffers allowing data propagation. When in boundary scan mode, scan data can be captured from or loaded onto the bus.

## **JTAG Test Software**

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The software available at CERN, from JTAG technologies generates test vectors and programming vectors for boundary scan hierarchical systems as the one presented before. This software is divided into packages that allow the generation of the test vectors and the analysis of the results obtained. The packages are succinctly described next.

### **1 - Test Development Package**

Automatic Pattern Generator for testing the boundary scan infrastructure, the board Interconnections and the logic clusters.

The BS Infrastructure is the chain of boundary scan circuits that compose the board. Several tests are automatically generated to test the chain.

The board interconnections are interconnections involving pins of BS circuits. The generator tools use the board netlist, BSDL file of each BS circuit and the Connection file (with the hierarchical description of the system) to generate the test programs. Additional information concerning the board circuits may be necessary for generating certain tests.

Clusters are blocks of non-boundary scan logic that can be functionally tested using the access provided by the BS cells in the BS circuits for input and output. These clusters can be automatically tested.

### **2 - PLD Development Package**

Package for development of BS files for in-circuit programming of PLDs and FPGAs using the boundary scan infrastructure. This package uses a programming file generated by the PLD and FPGA development station, the board netlist, and the BSDL files to create a boundary scan programming file. Most families of circuits are supported (Altera, Xilinx, etc.). The generation process and the programming file format depend of the family of the circuit to program.

### **3 - Boundary Scan Diagnostics**

Errors in the boundary scan infrastructure and in the board interconnections can be diagnosed using a diagnostics tool included in the software.

## Boundary Scan References

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