HTR Status

CMS HCal meeting at FIT
Feb. 7-9, 2002

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Readout - 9U VME crate

**BIT3-like** 6U board
- Commercial module
- Slow monitoring

**FanOut** board
- FanOut of TTC stream
- FanOut of RX_CK & RX_BC0

**HTR (HCAL Trigger and Readout)**
- FE-Fiber input
- TPs output to HEX-SLB
- DAQ/TP Data output to DCC
- Spy VME output

**DCC (Data Concentrator Card)**
- Input from HTRs
- Output to DAQ & TrigDAQ
- Spy VME output
**HCAL TRIGGER and READOUT Card**

- **Front panel:**
  - FE-data Inputs: 16 digital serial fibers, 3 QIE channels per fiber
  - Timing Inputs: clock, BC0, etc (LVDS; RJ-45 connector)
  - DAQ-data Output to DCC: 2 Channel Links

- **FPGA logic:**
  - L1/Trigger Path: Trigger primitive preparation and transmission
  - L2/DAQ Path: Waiting for L1 Decision, filtering or BCID (?), transm. to DCC
  - VME Interface, slow control

- **Transition board (HEX-SLB):**
  - Receives Trigger Primitives via standard P2/P3 (280 Mb/s // LVDS)
  - Holds 6 SLB daughterboards
  - Transmission with Vitesse/shielded twisted pair

Feb 2002
## Changes Demonstrator $\rightarrow$ Prototype

<table>
<thead>
<tr>
<th>FE input</th>
<th>Glink @ 800 Mb/s $\rightarrow$ GE @ 1.6 Gb/s</th>
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</thead>
<tbody>
<tr>
<td># of QIE-channels</td>
<td>16x2 $\rightarrow$ 12x3 $\rightarrow$ 16x3</td>
</tr>
<tr>
<td>Timing input</td>
<td>TTC board $\rightarrow$ TTC chip</td>
</tr>
<tr>
<td>Core logic</td>
<td>Altera $\rightarrow$ Xilinx</td>
</tr>
<tr>
<td>Trigger output</td>
<td>$\rightarrow$ on the new Transition board</td>
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<tr>
<td>Form factor</td>
<td>6U $\rightarrow$ 9U</td>
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## Things that remain unchanged

| DAQ output       | Channel Link                              |
HTR Pre-Prototype

Received: Nov 2001
Included: Optical input, Xilinx FBGA logic, DAQ output, VME.
Not included: TTC input, Trigger output.

IMPLEMENTATION DETAILS:
• Hi-Speed differential lines: matched in single-end $Z_c$ and length (20 mils);
  max length ~ 5 inches; no vias (TI approach).
• ‘Thermal land’ underneath the TI chips.
• Separate VDD and VDDA planes + filters.
• Parallel data lines: 80 Mb/s, minimized length, no vias, serial dumping resistor.
• Clever pin-assignement on Xilinx
Zoom on Pre-Prototype lay-out
Results from testing

Xilinx FBGA and VME circuitry passed basic testings.

Optical input not working.

These changes were unsuccessfull:

- Shortening the high-speed path (Connecting the optical receiver directly to the TI deserializer).
- Using different optical receivers.
- Providing a better reference clock.
- Playing with analog levels and decoupling capacitors.
- Reduce noise on VDD (all FPGAs unprogrammed).
Possible reasons for failure

• Wrong footprint for TI part (bigger than the chip)
  → company refused to assemble TI part
  → in-home assembly: no temperature control

• Geometry of $V_{DDA}$ and $V_{DD}$ planes ⇒ digital noise

• Reference clock without PLL driver ⇒ jitter
Link-only board

All mentioned reasons were eliminated. The board includes also Tracker-like and electrical inputs.
Link-only board

All mentioned reasons were eliminated.
The board includes also Tracker-like and electrical inputs.

Testing Results: works (only with controlled assembly)

- Jitter
- Max offset on frequency

Need more investigation (with FNAL)
HTR prototype

Lay-out 90% complete according to the baseline scheme and test results of the Link-only board.

TTCrx parts needed

Submission in March?
Data Paths

DAQ-path: we have a basic firmware:

• 24 channels/FPGA
• 10 samples/event (raw QIE data)
• Max trigger rate (peak) ~ 150 kHz
• Adjustable L1-latency pipeline
• No Zero-Suppression
• No BCID

Next steps:
• Improve sustainable trigger rate
• Zero-Suppression on raw data?
• BCID

Trigger Path: contribution from Princeton?
Near future

• Investigation timing issues → applied to prototype design

• Definition of the DAQ-path for the Test Beam

• Definition of the timing requirements for the Test Beam

• Integration with the Fanout board and FE board

• Definition of backplane (for Transition Board power)

• HO requirement on our trigger path/link

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Pre-production very short. 
Test bench before production? 
Slice Test I with pre-production?