Requirement on DAQ system for TB 2002
From off-line discussion at FIT: Eric, Tullio, etc

• Collect data from ~ 300-500 QIE-channels
• Record 10 QIE time samples per channel in response to trigger
• Trigger arrives less than 6.4us after data (adjustable latency)
• Process TTC commands for reset, start_run, stop_run
• Testing feature via VME

Features not-supported

• No L1-trigger path
• No CapID check, zero-suppression, filtering, BX IDentification
• No fiber-to-fiber alignment

Data_out[0-15] = { Mantissa, Range, CapIDs, Link_DV, Link_ER, Channel_ID }
HTR FPGA for Test Beam 2002 - Basic Data Path

From link

Rx_Clk 80 MHz

Syncro Stage 1

Rx_Clk 80 MHz

Syncro Stage 8

System Clock x 2

2 → 3 Demux

Latency pipeline

Derand Buffer

Latency pipeline

Derand Buffer

Latency pipeline

Derand Buffer

Latency pipeline

Derand Buffer

Latency pipeline

Derand Buffer

Latency pipeline

Derand Buffer

payload[15:0]

Data Buffer

Format Hamming and Parity

OUTPUT to DCC
HTR FPGA for Test Beam 2002 - testing features

From VME

DataTrig TestFIFO

From link

Syncro Stage 1
Rx_Clk 80 MHz

Syncro Stage 8
Rx_Clk 80 MHz

2 → 3 Demux
Input Spy FIFO
Latency pipeline
Derand Buffer

Latency pipeline
Derand Buffer

Latency pipeline
Derand Buffer

Latency pipeline
Derand Buffer

Latency pipeline
Derand Buffer

Latency pipeline
Derand Buffer

Latency pipeline
Derand Buffer

Latency pipeline
Derand Buffer

24 input Channel Mux
payload[15:0]

Derand Buffer

payload[15:0]

Data Buffer
Format Hamming and Parity

Output Spy FIFO

VME

OR

Test_L1A

TTCrx_L1A

OUTPUT
to DCC
Jitter on HTR
Jitter on HTR

Goal:
Jitter on HTR

X-tal PLL → ~20ps pk-pk
Diff PECL

Narrow range of frequency

Jitter spec 40 ps pk-pk

RefCK1
Link rx 1

RefCK2
Link rx 2

RefCK16
Link rx 16
Jitter on HTR

X-tal PLL
~20ps pk-pk
Diff PECL

Distribution network

Link rx 1
RefCK1

Link rx 2
RefCK2

Link rx 16
RefCK16

Jitter spec
40 ps pk-pk
Jitter on HTR

Dasy-chain: does not work because of capacitive load

Jitter spec 40 ps pk-pk

X-tal PLL

~20ps pk-pk

Diff PECL

RefCK1

Link rx 1

RefCK2

Link rx 2

RefCK16

Link rx 16
Jitter on HTR

- X-tal PLL
  - 20ps pk-pk
  - Diff PECL

  Fan-out: increase jitter to ~100 ps pk-pk (either PLL-based or not)

  - RefCK1
    - Link rx 1
  - RefCK2
    - Link rx 2
  - RefCK16
    - Link rx 16

Jitter spec
- 40 ps pk-pk
Jitter on HTR

Jitter spec
40 ps pk-pk

100ps pk-pk

normal PLL

CMOS

RefCK1
Link rx 1

RefCK2
Link rx 2

Fan-out:
increase jitter to
~ 100 ps pk-pk
(either PLL-based or not)

RefCK16
Link rx 16

Broad range of frequency